REMARKS/ARGUMENTS

The Applicant acknowledges, with thanks, receipt of the Office Action mailed July 14, 2004. Claims 1-41 are pending. Claims 1-41 stand rejected. By this amendment, claims 1, 6, 10, 15, 19 and 24 have been amended. Claims 28-41 have been canceled without prejudice or disclaimer.

Claim 1 has been amended to recite formatting the data portion of a data packet by a media access control layer processor (MAC processor) while the packet is stored in a first memory device and executing a single processor instruction by the MAC processor to a portion of the data portion of the packet from the first memory device to a main memory device. Formatting the data portion of the frame by the MAC processor is not new matter as it is disclosed in the original specification on page 11, lines 24-26. Claims 10 and 19 have been similarly amended and include means and/or devices configured for performing the aforementioned formatting function.

Claim 6 has been amended to recite processing the header portion of the packet by a MAC processor while the packet is stored in the first memory device and executing a single processor instruction on the MAC processor to move a portion of the packet from the first memory device to another memory. Processing the header portion of the frame by the MAC processor is not new matter as it is described on page 12, lines 12-14 of the original specification. Claims 15 and 24 have been similarly amended and include means and/or devices configured for performing the aforementioned processing function.

Executing a single processor instruction, as opposed to a single program instruction, is not new matter as it is disclosed in the original specification from page 10 line 15 to page 11 line 5. The processor moving a portion of the stored packet from the first memory to the second memory is not new matter as it is disclosed in the original application (see for example original claim 1).

Applicant would like to acknowledge, with thanks, the telephone interview conducted with the Examiner, Applicant and Applicant's representative. The Sandorfi reference was discussed, no agreement was reached.

I. Rejection of claims 1-41 under 35 U.S.C. § 103

Claims 1-41 were rejected under 35 USC § 103 as being obvious over the combination of US Patent No. 5,768,530 to Sandorfi (hereinafter "Sandorfi") and US Patent No. 5,452,291 to Eisenhandler (hereinafter "Eisenhandler"). Claims 28-41 have been canceled. For the reasons that will set forth below, claims 1-27 as now amended should be patentable over the combination of Sandorfi and Eisenhandler.

Claims 1, 10 and 19 as now amended, recite formatting the data portion of a packet by a media access control layer processor (MAC processor) while the packet is stored in a first memory device and executing a single processor instruction by the MAC processor to transfer a portion of the packet from the first memory device to a main memory. To summarize, the MAC processor both formats the data portion of the packet and uses a single processor instruction to transfer a portion of packet from the first memory to another memory. Furthermore, new claim 42 recites that the single instruction repeatedly executed until the entire packet is transferred. In contrast, an object of Sandorfi is "to provide an architecture for an interfacing circuit that eliminates any need for a processor to control interface operations" (col. 2, lines 44-46), whereas the present invention as claimed uses a processor to control interface operations. Furthermore, referring to Fig. 4, Sandorfi uses a "frame processing circuit 10 that receives the incoming information frame and divides each frame into a header portion for transfer into a received header FIFO (first in, first out) buffer 51 and a data portion for transfer into a received data FIFO buffer 52" (col. 5, lines 63-67). The claims as now amended recite that the data portion and header portion are stored together in a first memory, not divided into separate FIFO buffers as described in Sandorfi. Because Sandorfi divides the header and data portions of the

packet into separate FIFO buffers, Sandorfi cannot format the data portion of the packet which is stored with the header portion in the first memory.

Furthermore, Sandorfi also teaches that a "bypass" code can be used "to modify the recipient sequence manager 60 so that it responds to an appropriate value of the "bypass" code by conditioning the DMA transfer control 220 to transfer data directly from the data FIFO buffer 52 to the system memory 15M" (col. 14, lines 36-43). Recall from previous paragraph that only the data portion is stored in FIFO buffer 52, the data portion is stored in FIFO buffer 51. By contrast, the claims as now amended recite the data portion is formatted by the MAC processor, and a portion of the packet, which contains both the data and header portions are transferred from the first memory to the other memory, and that the transfer is performed by the processor, not by a DMA transfer control. An advantage of the present invention as now claimed is that because the software on the MAC processor performs the transfer, the firmware has the ability to react to the data stream on a timely basis, and perform functions such as formatting the data portion of the stream, unlike DMA which merely performs a block transfer.

Similarly, claims 6, 15 and 24 recite processing the header portion of the packet by a MAC processor while the packet is stored in the first memory device and executing a single processor instruction on the MAC processor to move a portion of the packet from the first memory device to another memory. In other words, the MAC processor performs both operations of processing the header portion and moving a portion of the data packet containing both the data and header portion from the first memory to another memory.

In contrast, an object of Sandorfi is "to provide an architecture for an interfacing circuit that eliminates any need for a processor to control interface operations" (col. 2, lines 44-46), whereas the present invention uses a processor to control interface operations. Furthermore, referring to Fig. 4, Sandorfi uses a "frame processing circuit 10 that receives the incoming information frame and divides each frame into a header portion for transfer into a received

header FIFO (first in, first out) buffer 51 and a data portion for transfer into a received data FIFO buffer 52" (col. 5, lines 63-67). The claims as now amended recite that the data portion and header portion are stored together in a first memory, not divided into separate FIFO buffers as described in Sandorfi. In addition, because Sandorfi divides the header and data portions of the packet into separate FIFO buffers, Sandorfi does not process the header portion of the packet which is stored with the data portion in the first memory.

Furthermore, Sandorfi also teaches that a "bypass" code can be used "to modify the recipient sequence manager 60 so that it responds to an appropriate value of the "bypass" code by conditioning the DMA transfer control 220 to transfer data directly from the data FIFO buffer 52 to the system memory 15M" (col. 14, lines 36-43). Recall from previous paragraph that only the data portion is stored in FIFO buffer 52, the data portion is stored in FIFO buffer 51. By contrast, the claims as now amended recite the header portion is processed by the MAC processor and both the data and header portions are stored in the first memory and a portion of the packet which contains both the header portion and the data portion is transferred to the other memory, and that transfer is performed by the processor, not by a DMA transfer control. An advantage of the present invention as now claimed is that because the software on the MAC processor performs the transfer, the firmware has the ability to react to the data stream on a timely basis, such as by processing the header, unlike DMA which merely performs a block transfer of data.

The Examiner relies on Eisenhandler for showing receiving a wireless signal from a radio frequency physical layer, which does not remedy the aforementioned deficiencies in Sandorfi.

Thus for the reasons set forth above, neither Sandorfi or Eisenhandler, taken alone or in combination, teach, suggest or show all of the elements of claims 1, 6, 10, 15, 19 and 24. Therefore, these claims should now be in condition for allowance. Furthermore, claims 2-5 and 42, 7-9, 11-14, 20-23 and 25-27 are directly dependent from claims 1, 6, 10, 15, 19 and 24

respectively and therefore, contain each and every element of claims 1, 6, 10, 15, 19 and 24. Thus, for the reasons set forth above for claims 1, 6,, 10, 15, 19 and 24, claims 2-5 and 42, 7-9, 11-14, 20-23 and 25-27 should now be in condition for allowance. Therefore, for the reasons just set forth, claims 1-27 should be in condition for allowance.

In view of the foregoing, it is respectfully submitted that the present application is now in proper condition for allowance. If the Examiner believes there are any further matters which need to be discussed in order to expedite the prosecution of the present application, the Examiner is invited to contact the undersigned.

If there are any fees necessitated by the foregoing communication, please charge such fees to our Deposit Account No. 50-0902, referencing our Docket No. (72255/02661).

Respectfully submitted,

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